Keynote:

TERAFLUX: Ideas for the Future Many-Cores

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Abstract

Recent Silicon advances promise to keep "Moore's Forecast" true for at least this decade. In numbers, one TERA (10^12) transistors in a single chip or package will be available, posing three major challanges for future computing systems: i) how to efficiently program these systems? ii) which architecture would lead to a managable complexity? iii) how do we keep the system reliable? The TERAFLUX project (http://teraflux.eu - with a total cost of about 7.5 M-Euro) allows 10 Academic and Industrial partners to join forces in order to propose a holistic solution able to address the three above challanges.

Many proposals for future many-core system are gaining attention nowadays: CUDA based systems contain already 512 cores per chip, while x86 multi-core processors arrived already to 12 cores. TERAFLUX leverages Dataflow Parallelism to reach power efficiency, reliability, efficient parallel programmability, scalability, data bandwidth.

Dataflow is exploited both at task level and inside the threads, to offload accelerated codes, to localize the computation, for managing the fault information with appropriate protocols, to easily migrate code to the available/working components and to respect the power/performance/temperature/reliability envelope, to produce a more predictable behavior, to efficiently handle the parallelism and have an easy and powerful execution model.

A special challange is the evaluation of such system comprising a target of at least 1000 cores. Our simulation infrastructure relies on the COTSon simulator provided by HP-Labs (TERAFLUX partner). One more contribution of this project is to provide an updated COTSon-based TERAFLUX simulator as an Open-Source project.

Biography

Roberto Giorgi is an Associate Professor at Department of Information Engineering, University of Siena, Italy. He received his PhD in Computer Engineering and his MS in Electronics Engineering, Magna cum Laude both from University of Pisa, Italy. He is the coordinator of the European Project TERAFLUX in the area of Future and Emerging Technologies for Teradevice Computing. He is participating in the European projects HiPEAC (High Performance Embedded-system Architecture and Compiler) and SARC (Scalable ARChitectures), ERA (Embedded Reconfigurable Architectures). He took part in ChARM project, developing software for performance evaluation of ARM-processor based embedded systems with cache memory, for VLSI Technologies Inc., San Jose (which later became Philips Semiconductor and then NXP). He has been IEEE Judge for the IEEE-CSIDC (Computer Society International Design Competition). He led the project "Bluesign Translator", which received a 5th worldwide prize by IEEE, ABB, AMD, EMC, HP, Intel, Lucent, Microsoft, Motrola, SAIC, Sun, and received the FORUM-P.A. prize by the Italian Ministry of Technological and Scientific Innovation, CNIPA, ASPHI, Ericsson as absolute winner in the category of "actions for the social integration of disadvantaged actions through ICT". He has been selected by the European Commission as an independent expert for evaluating the European Project SHAPES (Scalable Software Hardware Architecture Platform for Embedded Systems). He is co-author of more than 70 scientific papers. His current interests include Computer Architecture themes such as Embedded Systems, Multiprocessors, Memory System Performance, Workload Characterization. He is member of the HiPEAC Network of Excellence (High Performance Embedded-system Architecture and Compilation). He is member of ACM and Senior Member of the IEEE, IEEE Computer Society.